

CLAIMS

We claim:

1 1. A method of forming an integrated chip package, comprising
2 the steps of:

3 providing a first substrate and a second substrate, each
4 having conductive pads thereon;

5 applying a mask to at least one of the first and second
6 substrates, wherein the mask has a plurality of non-circular
7 openings having a first dimension and a second dimension, such
8 that the conductive pads are not covered by the mask in the
9 direction of the first dimension and partially covered by the
10 mask in the direction of the second dimension; and

11 providing a reflowable material between the conductive pads
12 of the first and second substrates.

1 2. The method of claim 1, wherein the first dimension of the
2 elongated non-circular openings is greater than the second
3 dimension of the non-circular openings.

1 3. The method of claim 1, wherein the first dimension of the
2 non-circular openings is selectively oriented in the direction of
3 highest stress for each interconnection formed from the
4 reflowable material within the integrated chip package.

1 4. The method of claim 1, wherein the non-circular openings of
2 the mask are elliptical.

1 5. The method of claim 1, wherein the conductive pads are
2 circular.

1 6. The method of claim 5, wherein the conductive pads are
2 copper.

1 7. The method of claim 1, wherein the mask comprises a non-
2 wettable material.

1 8. The method of claim 7, wherein the mask comprises an epoxy.

1 9. The method of claim 1, wherein the first substrate is a chip
2 carrier.

1 10. The method of claim 1, wherein the second substrate is a
2 printed circuit board.

1 11. The method of claim 1, wherein the reflowable material is
2 solder.

1 12. The method of claim 1, wherein a plurality of traces are
2 mounted between the non-circular openings of the mask.

1 13. The method of claim 1, wherein the integrated chip package
2 is a Ball Grid Array package.

1 14. An integrated chip package comprising:
2 a first substrate and a second substrate, wherein at least
3 one of the first and second substrates includes a plurality of
4 partially captured pads; and
5 a plurality of interconnections between the first and second
6 substrates.

1 15. The integrated chip package of claim 14, wherein the
2 plurality of partially captured pads are formed by a mask having
3 elongated non-circular mask openings.

1 16. The integrated chip package of claim 15, wherein the
2 elongated non-circular mask openings have a first dimension and a
3 second dimension.

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1 17. The integrated chip package of claim 16, wherein the first
2 dimension of the elongated non-circular mask openings is greater
3 than the second dimension of the elongated non-circular mask
4 openings.

1 18. The integrated chip package of claim 16, wherein the first
2 dimension of the elongated non-circular mask openings is
3 selectively oriented on the substrate in the direction of highest
4 stress within each interconnection.

1 19. The integrated chip package of claim 14, wherein the
2 interconnections have a combination of mask-defined and pad-
3 defined solder joint profiles.

1 20. A substrate having a plurality of conductive pads and a mask
2 thereon, wherein the mask has a plurality of openings having a
3 first dimension larger than the conductive pad, and a second
4 dimension smaller than the conductive pad.

1 21. The substrate of claim 20, wherein the conductive pads are
2 circular.

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1 22. The substrate of claim 20 wherein the first dimension of
2 the openings is greater than the second dimension of the
openings.

1 23. The substrate of claim 22, wherein the first dimension of
2 the openings is selectively oriented in the direction of highest
3 stress within a plurality of interconnections formed within the
4 openings of the substrate.

1 24. An integrated circuit mask having a plurality of elongated
2 non-circular openings therein, wherein the openings have a first
3 dimension greater than a second dimension, such that the first
4 dimension of the openings coincides with the direction of the
5 highest stress within the integrated circuit.

1 25. The integrated circuit mask of claim 24, wherein the mask
2 comprises a non-wettable material.

1 26. An integrated circuit interconnection, wherein the
2 interconnection is mask-defined in a first direction and pad-
3 defined in a second direction.

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